

High-Performance and Area-Efficient Stacked Transformers for RF CMOS Integrated Circuits

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Abstract □ A solenoid layout technique is used to increase the magnetic coupling between the coils in multi-level spiral transformers. Using this technique, transformers with the following performance are measured: (a) magnetic coupling with coupling factor $k>0.95$ and insertion loss s_{21} better than 0.8dB at 5GHz; (b) self-resonant frequency $f_{res}>15$ GHz with peak $Q>10$. The effect of high and low resistive substrates is discussed with measured results. Using this structure, the size of the transformer can be reduced from 50 to 400%.

I. INTRODUCTION

Monolithic transformers [1] have been used extensively in RF blocks to improve circuit performances. Not only they have the properties of inductors that can be used for frequency tuning and dc short, transformers are particularly useful for signal coupling and impedance transformation. These two properties provide significant advantage for low-voltage design as demonstrated in [2][3]. Similar to inductors, besides limited choice of inductance and poor Q compared to off-chip components, one major drawback of transformers is the large area required for monolithic realization. Furthermore, their large dimensions often enforces long interconnects for routing which introduces extra energy loss to the substrate. Despite cheaper cost compared to off-chip component, the monolithic inductive elements are considered to be expensive for their large area consumption. This cost issue is especially pronounced for large RF systems such as MIMO [4] where multiple transceivers are required.

In this paper, a stacking layout technique is introduced to increase the magnetic coupling between the spirals. When applied to transformers, the improvement in magnetic coupling reduces insertion loss, and compact high-frequency transformer beyond 10GHz can be realized. Compared to published transformers [1]-[3][6][7], the transformer size can be reduced from 50 to 400%.

All the passives presented in this paper are implemented in an 0.12 μ m SOI CMOS process [8] with 8 levels of standard digital copper metalization (Table I) with high-resistive substrate (HRS) of resistivity between 100 to 1000 Ω -cm. Test structures in low-resistive substrate (LRS) with 10 Ω -cm resistivity are also measured for performance comparison.

TABLE I. Metalization parameters

metal level	distance to substrate d [μ m]	metal thickness [μ m]
M8	10.6	1.2
M7	7.8	1.2
M6	5.8	0.6
M5	4.6	0.6

II. TRANSFORMERS

Monolithic transformers have been used extensively in RF circuits. Depending on the circuit application and frequency of operation, transformer design can be varied quite drastically. For voltage coupling (Fig. 1a and b), the transformer is optimized for voltage transfer and magnetic coupling. For a balun (Fig. 1c) that provides conversion between balanced and unbalanced circuits, differential balancing and impedance transformation are the primary considerations. Meanwhile, for current driven circuit, small signal current gain h_{21} is the most important parameter (Fig. 1d).

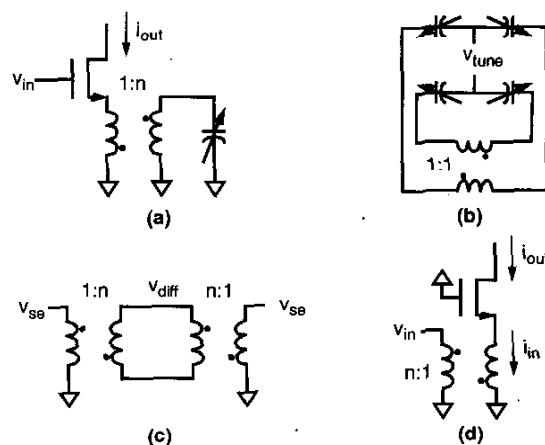


Fig. 1. Transformer applications: (a) image-reject filter (LNA) [3]; (b) high- Q resonator (VCO) [6]; (c) single-ended (s.e.) to differential conversion (balun); (d) voltage-controlled current source (mixer) [1].

III. DESIGN AND MEASUREMENT

In this paper, transformer structure is defined by number of coil turns n , number of metal layers m and outer diameter OD . Minimum spacing is used between metals, and all transformers have metal width w set to 15 μm with minimum metal width of 4 μm . Two-port s-parameters are used to measure the transformer, and several parameters are extracted to characterize the device. Primary and secondary self inductances (L_p and L_s), associated Q and self-resonant frequency f_{res} are used to characterize the impedance of the transformer. Meanwhile, three figures of merits are used to measure the magnetic coupling between the coils: (a) transmission coefficient

$$s_{21} = s_{12} \quad (1)$$

where s_{ij} are 2-port s-parameters; (b) coupling factor k

$$k = \frac{M}{\sqrt{L_p L_s}} \quad (2)$$

where M is the mutual inductance, which can be extracted from the imaginary part of z-parameter z_{21} (or z_{12}); (c) small signal current gain h_{21}

$$h_{21} = \left| \frac{y_{21}}{y_{11}} \right| \quad (3)$$

where y_{ij} are 2-port y-parameters.

A. Highly Coupled Stacked Transformer

A 1:1 transformer can be employed where circuits required neither voltage nor current gain between the coupled signals, such as VCO resonator [6] or quadrature circuits [7]. It is also useful for low-voltage circuits where high-linearity is required. In both cases, the transformer is designed for the best magnetic coupling to reduce insertion loss. Conventionally, n greater than 4 is used to improve magnetic coupling. However, the increase in device dimension is not only costly but also degrades frequency performance due to substrate loss.

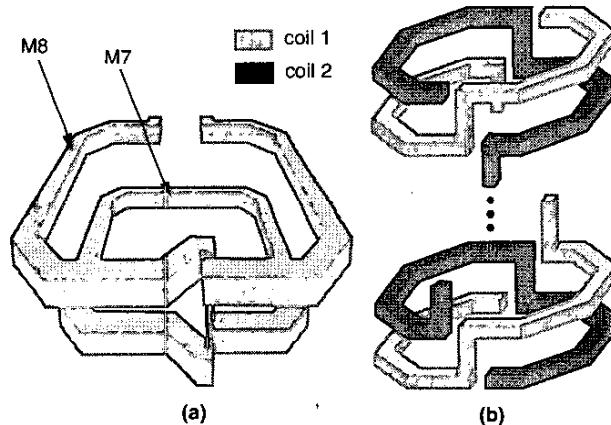


Fig. 2. Multi-level transformers: (a) stacked differential with 1 turn each level (only one coil is shown), and (b) solenoid single-ended with 0.5 turn each level.

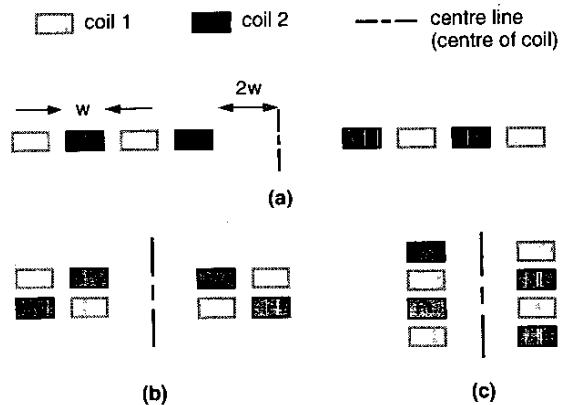


Fig. 3. Cross sections of transformer structures: (a) planer differential ($m=2$); (b) stacked differential ($m=2, n=2$); (c) solenoid single-ended ($m=4, n=2$)

If multi-level metal process is available (especially in digital process), stacking multiple layers of metal (Fig. 3) instead of using only one layer can reduce chip area and provide extra magnetic coupling. Consider the cross sections of transformers with $n = 2$ as shown in Fig. 3. Assume the innermost winding is two w away from the centre line, the area for (a) is $144w^2$, (b) is $64w^2$ and (c) is $36w^2$. Clearly, by stacking extra layers the chip area can be reduced by 50 to 400%.

Magnetic coupling between coil can also be improved through stacking compared to planer structure. Consider the magnetic field lines as shown in Fig. 4, with a spacing of $4w$ assumed for inner diameter of the transformer. First, the vertical spacing is usually smaller than the minimum spacing between metal, and therefore the coupling is tighter. For stacked differential transformer, besides the horizontal coupling as in the planer structure, additional vertical coupling reduces flux leakage, improving energy transfer between coils through mutual inductance. As for solenoid transformer, there are two types of configuration because it is single-ended driven as shown in Fig. 5. Compared to inverting configura-

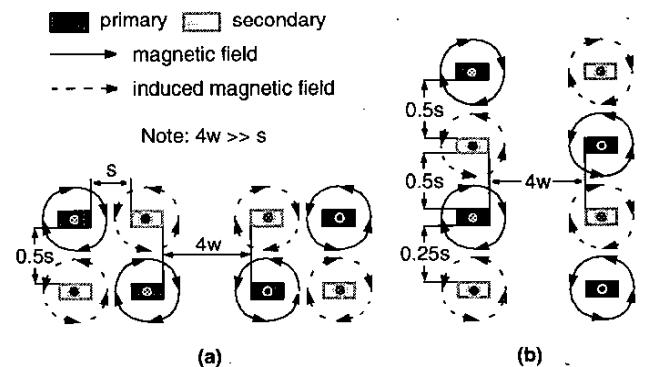


Fig. 4. Magnetic coupling of (a) stacked differential and (b) solenoid single-ended transformers for inverting configuration

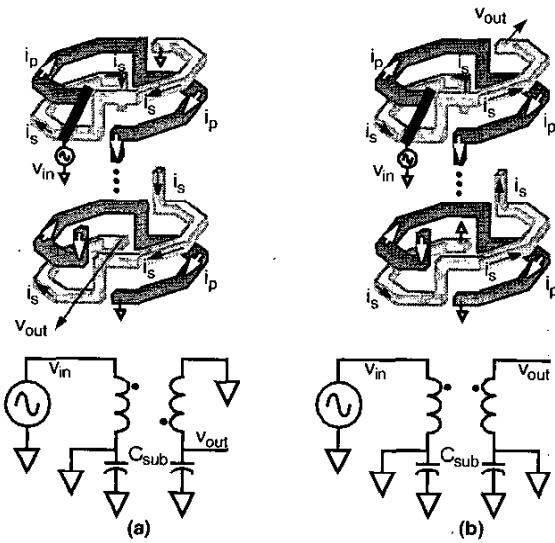


Fig. 5. (a) Inverting and (b) non-inverting configurations

tion, non-inverting configuration has better f_{res} because substrate capacitance C_{sub} of the secondary coil is grounded out (Fig. 5b). However, this ground also creates a virtual short circuit to the primary ground, forming a conductive plane. The magnetic field generated by the primary coil induces eddy current on this plane, reducing the magnetic coupling to the secondary coil. Therefore, non-inverting configuration has poorer magnetic coupling compared to the inverting one. One of the drawbacks of stacked transformer is that the distance between metal and substrate is reduced. Therefore, it is important to choose an appropriate ground or use HRS to reduce substrate loss.

Two types of transformers was fabricated and measured: $X1$ is the fully differential (Fig. 3b) with $n = 2$, $m = 2$ and $OD = 200 \mu\text{m}$ for balanced circuits, and $X2$ is the single-ended (Fig. 3c) with $n = 2$, $m = 4$ and $OD = 108 \mu\text{m}$ for minimum area consumption. Fig. 6 is the measured self-inductance and Q of both primary and secondary coil, and they are virtually the same, indicating the turn ratio is truly 1:1. Since the peak coupling occurs when the transformer is at resonant, the self-resonant frequency f_{res} represents the highest frequency for the transformer to achieve the lowest possible transmission loss. Therefore, unlike the inductor, the transformer can still be used if operated above f_{res} , except that the coupling changes from inductive (magnetic) to capacitive (electric). Transformer $X1$ has the lowest f_{res} because the area is the largest and hence greatest interwinding capacitance C_{int} . The f_{res} is expected to be higher when operated differentially. $X2$ is measured in both inverting (inv) and non-inverting (ninv) configurations. Non-inverting has a much higher f_{res} ($>15\text{GHz}$) due to low C_{int} and C_{sub} grounding as explained in Fig. 5b.

The magnetic coupling characteristics of the transformers are shown in and Fig. 7. For the differential transformer $X1$,

s_{21} of -0.8dB at f_{res} and k greater than 0.9 above 4GHz is measured. Meanwhile, $X2$ also has good s_{21} and k for both inverting and non-inverting configuration. Note that a differential transformer can be constructed by using two single-ended transformer, making $X2_{ninv}$ desirable for high frequency operation.

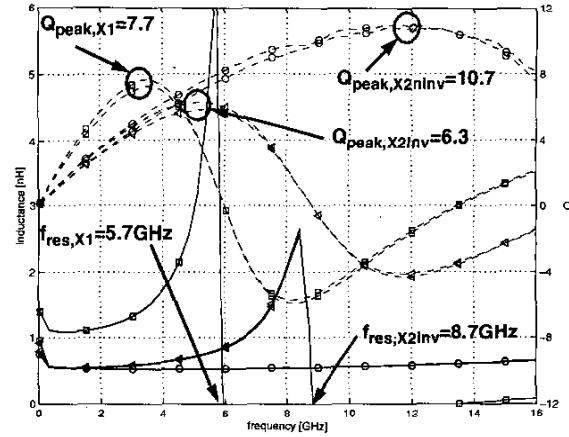


Fig. 6. Measured impedance of $X1$ (square), $X2_{inv}$ (triangle) and $X2_{ninv}$ (circle); solid line is inductance (L_1 , L_2), and dash line is quality factor (Q_p , Q_s).

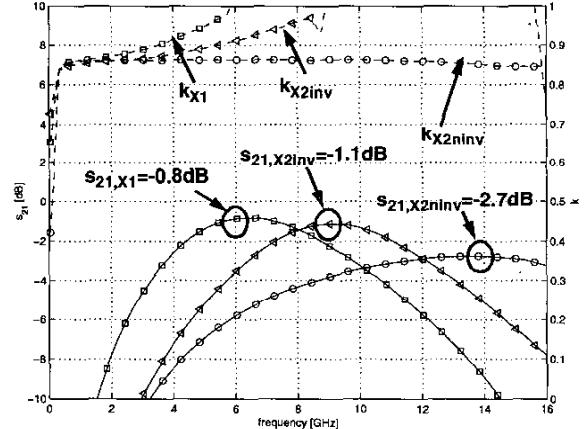


Fig. 7. Measured $|s_{21}|$ (solid line) and k (dash line) of stacked 1:1 transformers

The transformers are implemented in high-resistive substrate (HRS). However, as long as the metal layers are far away from the substrate (e.g., $X1$), substrate resistivity has only small effect on coupling performance (see next section). Therefore, this layout technique can be applied to low-resistivity substrate (LRS) as well. However, HRS reduces substrate loss, which is important if more turns and lower level metals are used to further reduce the size of the transformer (e.g., $X2$).

B. Substrate Resistivity

Unlike monolithic inductor, substrate resistivity usually has little effect to transformer characteristics if metal-to-sub-

strate distance d is much greater than the coil-to-coil spacing s . This is because while inductor has most of the energy lost to the substrate ground, transformer has the energy coupled from the primary to the adjacent secondary coil if the transformer metal layer is relatively far away from the substrate. Therefore, interwinding capacitance C_{int} is more significant than substrate capacitance C_{sub} . Since increasing substrate resistivity only reduces C_{sub} , C_{int} remains dominant so the effect on transformer characteristic is not significant.

To demonstrate this, a top-level metal only 2:1 transformer with $w = 15 \mu\text{m}$ and $OD = 250 \mu\text{m}$ as used in Fig. 1d is fabricated in both low and high resistive substrates (LRS and HRS). The impedance in inverting configuration is measured as shown in Fig. 8. The self-inductance are the same for both substrates, while HRS gives about 10% better Q and slightly higher f_{res} . Meanwhile, the coupling parameters s_{21} and h_{21} are effectively the same as shown in Fig. 8.

However, C_{sub} becomes significant if stacking is used because the lower metal is closer to the substrate and hence more susceptible to substrate loss. Therefore, in order to maintain high frequency response, HRS is necessary to prevent f_{res} from decreasing. HRS effectively moved the conductive ground plane further away from the transformer, reducing loss through eddy current and hence better magnetic coupling. This is especially important if the transformer is operating differentially.

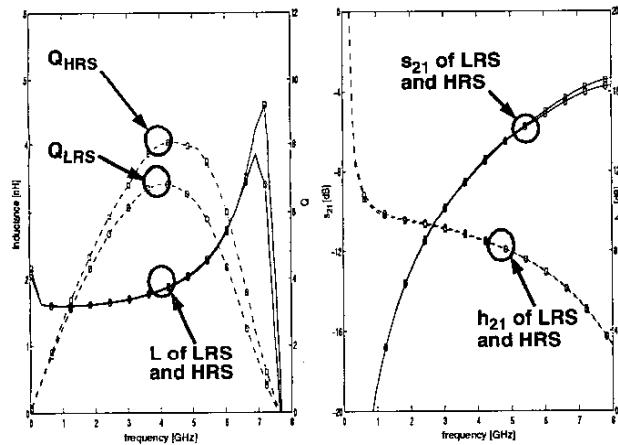


Fig. 8. (a) Measured self-inductance and Q and (b) s_{21} and h_{21} of 2:1 transformer in LHS (circle) and RHS (square)

IV. SUMMARY

By stacking multiple metal layers and using solenoid layout technique, measurement shows similar or better magnetic coupling and frequency response can be achieved. Meanwhile, the area can be reduced by 50 to 400% compared to published transformers as listed in Table II. Furthermore, HRS has a significant impact to a stacked differential transformer due to eddy current loss, while it has little influence if

TABLE II. Transformer comparison

Ref. cfg.	m	$n_1:n_2$	OD [μm]	d [μm]	L_p [nH] Q	s_{21} [dB]	k	f [GHz]	f_{res} [GHz]
[1] inv	1	4:4	400	5.75	8.5 NA	-2.25	0.82	2.5	4.9
[3] ninv	1	2:1	350	5.0	1.7 10	NA	0.54	5.0	10
[6]	1	6:6	250	3.0	5.5	NA	0.83	1.8	NA
[7]					9				
X1	2	2:2	200	7.8	1 7.0	-0.8 0.96	5.0	6.0	
X2	4	2:2	108	4.6	0.5 6.5	-1.1 0.9	5.4	8.5	
X2	4	2:2	108	4.6	0.5 10.5	-2.7 0.86	14	>15	
ninv									

metal layers are far away from the substrate. The micrograph of a 1:1 stacked differential transformer is shown in Fig. 9.

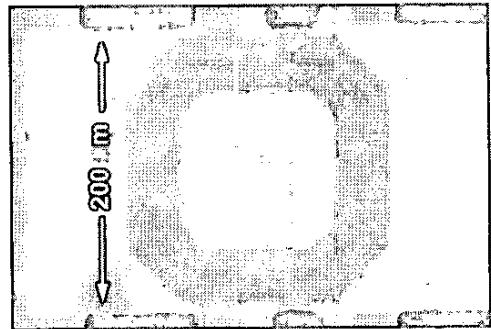


Fig. 9. Micrograph of 1:1 stacked differential transformer

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